University of California, Santa Barbara

Department of Electrical and Computer Engineering

ECE 152A – Digital Design Principles

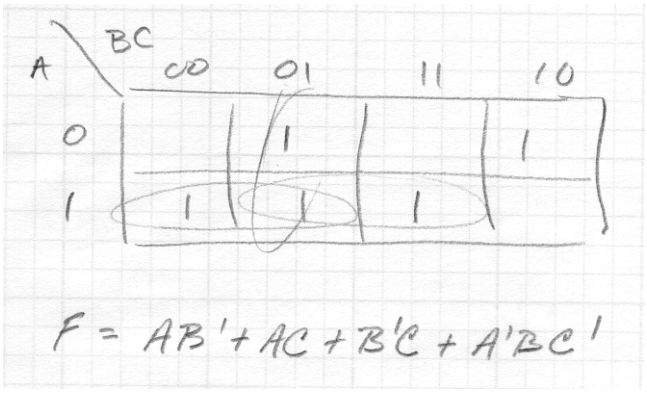
Homework #7 – Solution

Problem #1.

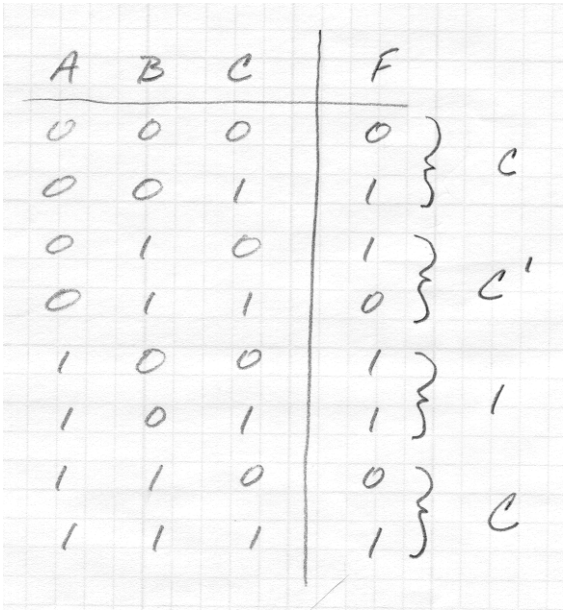
For the function below:

$$F(A,B,C) = \Sigma m(1,2,4,5,7)$$

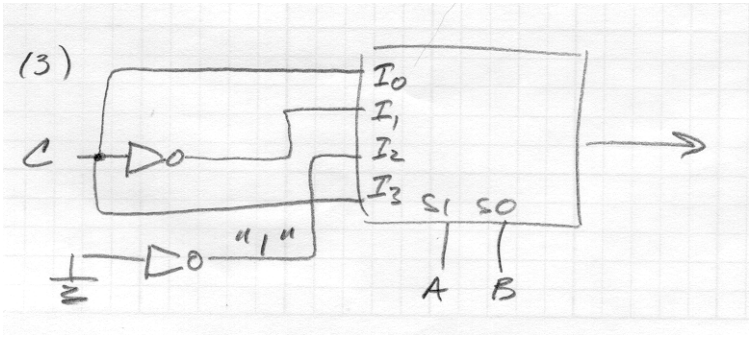
(1) Express the function in standard (minimized) sum of products form



(2) Construct a truth table for the function



(3) Implement the function with a four-to-one multiplexer:



(4) Using Shannon's expansion theorem, expand the function from part (1) above in terms of the variable A. Show all steps.

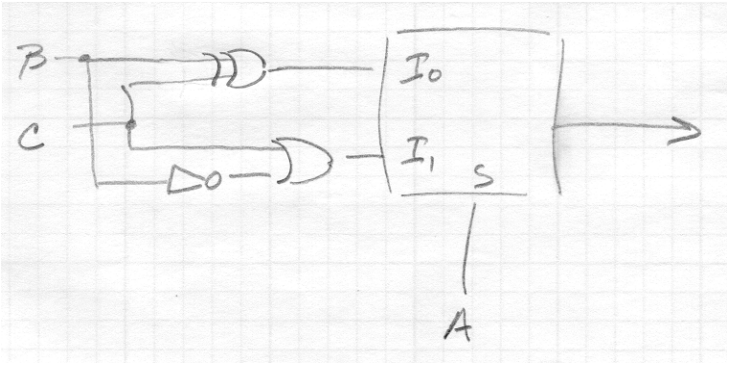
$$F = AB' + AC + B'C + A'BC'$$

$$= A(B' + C + B'C + (0)BC') + A'((0)B' + (0)C + B'C + BC')$$

$$= A(B' + C + B'C) + A'(B'C + BC')$$

$$= A(B' + C) + A'(B \oplus C)$$

(5) Implement the function with a two-to-one MUX and the minimum number of additional gates.



Problem #2.

In this problem you are to design a 4-bit barrel shifter (using TTL components) and determine its maximum frequency (minimum clock period) of operation.

Note: This problem consists of 4 parts. It is possible to do parts 3 and 4 without doing parts 1 and 2.

A barrel shifter allows rotating the contents of a register an arbitrary number of bits to the left or right. If the bits in this register are labeled A, B, C and D the operation of the barrel shifter is as shown below:

Shift Direction	Count	Register Contents			
Right	0	A	B	C	D
Right	1	D	A	B	C
Right	2	C	D	A	B
Right	3	B	C	D	A
Left	0	A	B	C	D
Left	1	B	C	D	A
Left	2	C	D	A	B
Left	3	D	A	B	C

The barrel shifter can be constructed using four D flip-flops and four 4:1 multiplexers, one on the D input of each flip-flop. Given a 3 bit control word indicating the direction (DIR: 0 = right and 1 = left) and count (CNT1, CNT0: 00 = 0, 01=1,10=2 and 11 =3), a combinational circuit (MUX select circuitry) generates the select inputs (S1 and S0) for the four multiplexers. The same S1 and S0 are applied to all four multiplexers, selecting the correct input to the D flip-flop.

The implementation of the barrel shifter will use 7474 D flip-flops, 74153 4:1 multiplexers and assorted NAND gates (7400, 7410, 7420, 7430). The relevant timing data is provided below.

7474

	SERIES 54/74	'70			'72, '73, '76, '107			'74			'109			'110			'111			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 54	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	Series 74	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}				−400			−400			−400			−800			−800			−800	μA
Low-level output current, I_{OL}				16			16			16			16			16			16	mA
Pulse width, t_w	Clock high	20			20			30			20			25			25			ns
	Clock low	30			47			37			20			25			25			
	Preset or clear low	25			25			30			20			25			25			
Input setup time, t_{su}		20↑			0↑			20↑			10↑			20↑			0↑			ns
Input hold time, t_h		5↑			0↓			5↑			6↑			5↑			30↑			ns
	Series 54	−55		125	−55		125	−55		125	−55		125	−55		125	−55		125	

7474

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'70			'72, '73 '76, '107			'74			'109			'110			'111			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Note 2	20	35		15	20		15	25		25	33		20	25		20	25		MHz
t_{PLH}	Preset (as applicable)	Q				50		16	25			25		10	15		12	20		12	18	ns
t_{PHL}		$\bar{Q}$				50		25	40			40		23	35		18	25		21	30	
t_{PLH}	Clear (as applicable)	$\bar{Q}$				50		16	25			25		10	15		12	20		12	18	ns
t_{PHL}		Q				50		25	40			40		17	25		18	25		21	30	
t_{PLH}	Clock	Q or $\bar{Q}$			27	50		16	25		14	25		10	16		20	30		12	17	ns
t_{PHL}					18	50		25	40		20	40		18	28		13	20		20	30	

¶ f_{max} ≡ maximum clock frequency; t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output.
NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

74153

switching characteristics, V_{CC} = 5 V, T_A = 25°C

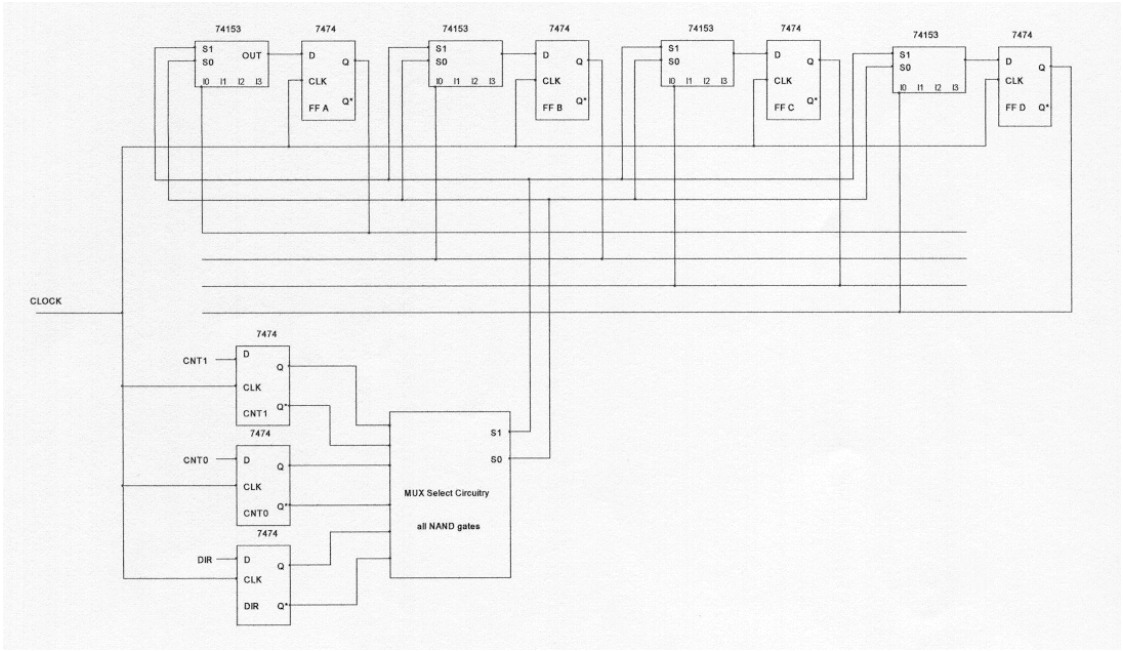
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L = 30 pF, R_L = 400 Ω, See Note 3		12	18	ns
t_{PHL}	Data	Y			15	23	ns
t_{PLH}	Select	Y			22	34	ns
t_{PHL}	Select	Y			22	34	ns

7400, 7410, 7420, 7430

switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'00, '10	C_L = 15 pF, R_L = 400 Ω		11	22		7	15
'04, '20			12	22		8	15
'30			13	22		8	15

1. Complete the schematic below by showing the connections between the outputs of the four flip flops and the inputs to the four multiplexers necessary to realize the barrel shifter. The multiplexers should get all four flip-flop outputs; the problem is which input gets which one (S1S0 = 00 : input = I0, 01 = I1, 10 = I2, 11 = I3). When there is no shift, the output of the flip-flop is fed back to the input of the same flip flop (as shown on the schematic).



SINCE DATA MUST REMAIN IN THE SAME ORDER (BUT ROTATED)

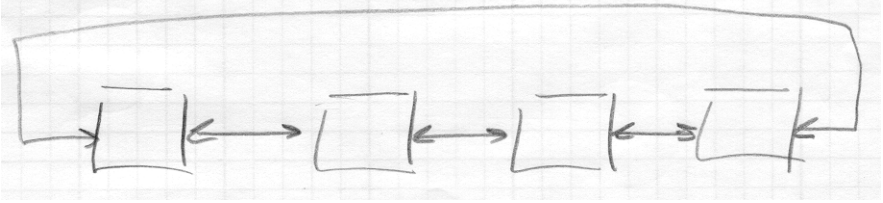
I_0 = FLIP-FLOP OUTPUT

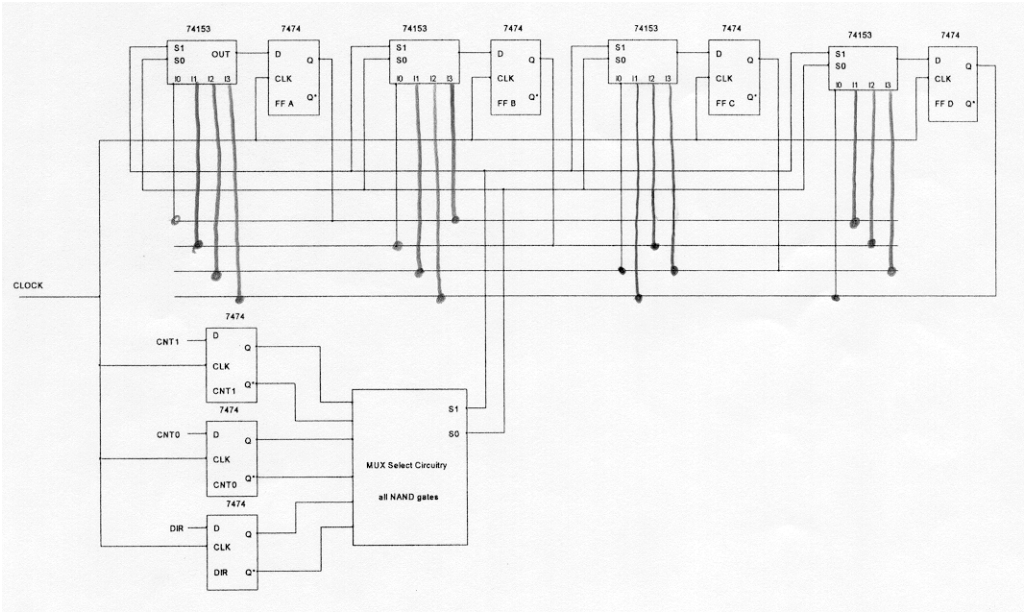
I_1 = ONE FF TO THE RIGHT

I_2 = TWO FF TO THE RIGHT

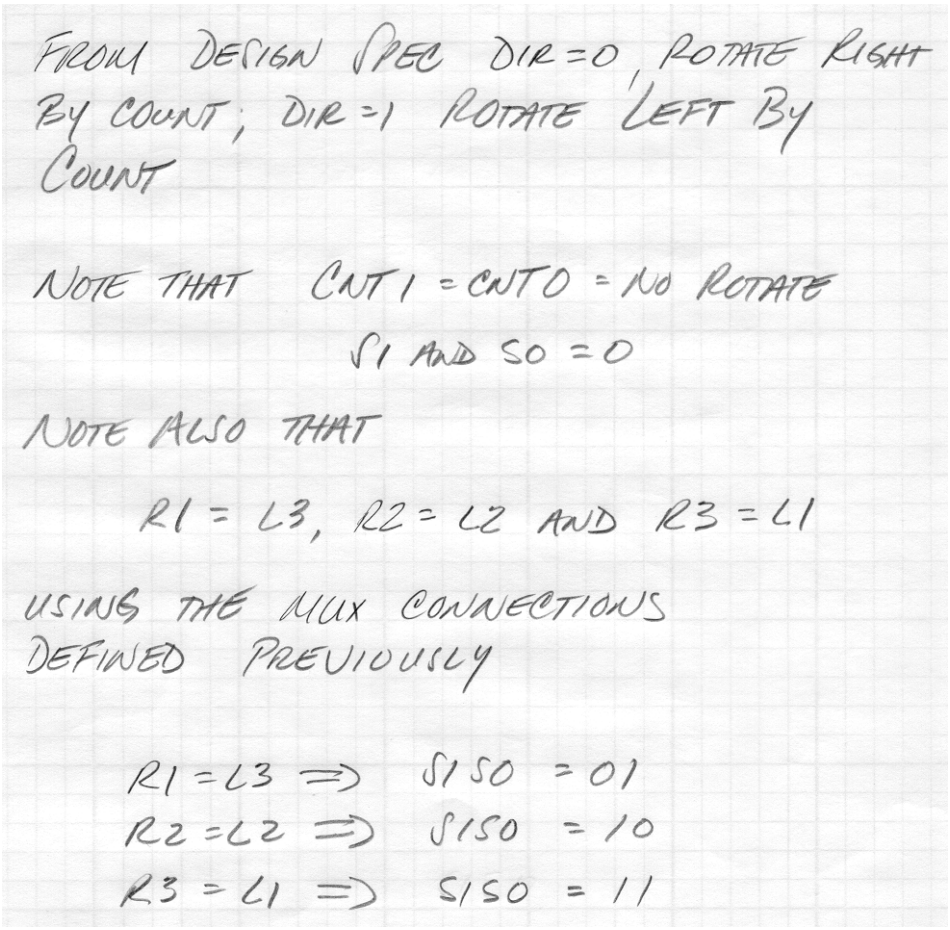
I_3 = THREE FF TO RIGHT

(ORDER TO THE LEFT ALSO WORKS)





2. The count and direction inputs are applied to the MUX select circuitry via 7474 D flip flops, hence both the true and complemented versions will be available (inverters not required). Based on the connections defined in part 1, design the MUX select circuitry using only NAND gates. Include Karnaugh maps and the minimized Boolean equations; you do not have to draw the schematic.



DIR \ CNT1 CNT0	00	01	11	10
0	0	0	1	1
1	0	1	0	1

$S_1 = DIR\,\overline{CNT1}\,CNT0 + \overline{DIR}\,CNT1 + CNT1\,\overline{CNT0}$

DIR \ CNT1 CNT0	00	01	11	10
0	0	1	1	0
1	0	1	1	0

$S_0 = CNT0$

NOTE: THE LOGICAL EQUATIONS WILL BE DIFFERENT BASED ON THE CONNECTIONS MADE IN PART 1 ... BUT THE TIMING WILL BE THE SAME

3. Determine the critical path in the design. (Note again: if you were unable to complete parts 1 and 2 above, you can assume that the MUX select circuitry can be realized via a 2-level NAND/NAND implementation).

THE CRITICAL PATH WILL BE THROUGH THE MUX SELECT CIRCUITRY, THROUGH THE MUX TO THE D INPUTS TO THE FLIP FLOPS

MUX SELECT CIRCUITRY:

- ALL NANDS, TWO LEVEL
- NO INVERTERS NEEDED
- ALL PATHS HAVE TWO INVERSIONS

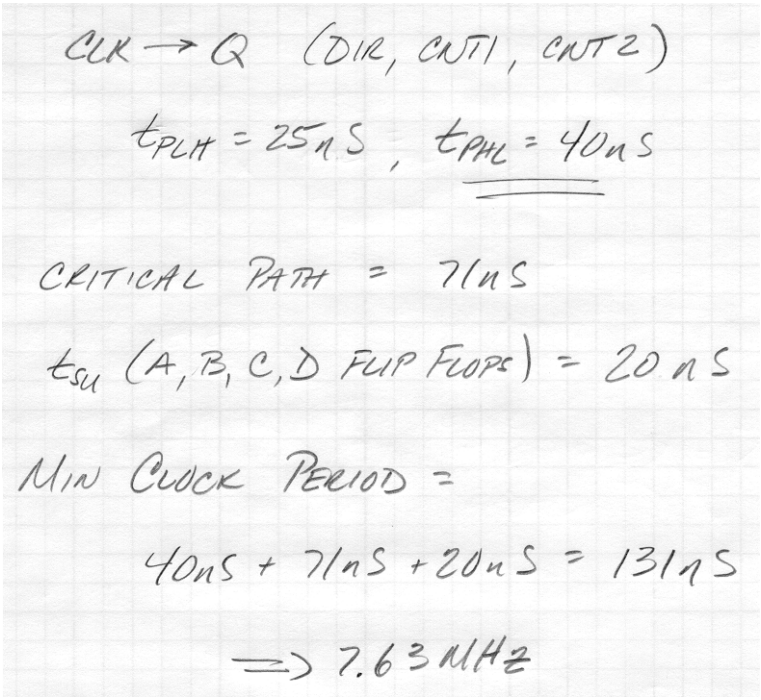
$\Rightarrow \Delta = t_{PLH} + t_{PHL} = 22 + 15 = 37nS$

MUX DELAY:

SELECT $\rightarrow$ Y, $t_{PHL} = t_{PLH} = 34nS$

$\therefore$ CRITICAL PATH $= 34 + 37 = 71nS$

4. Determine the minimum clock period for the design.



Problem #3.

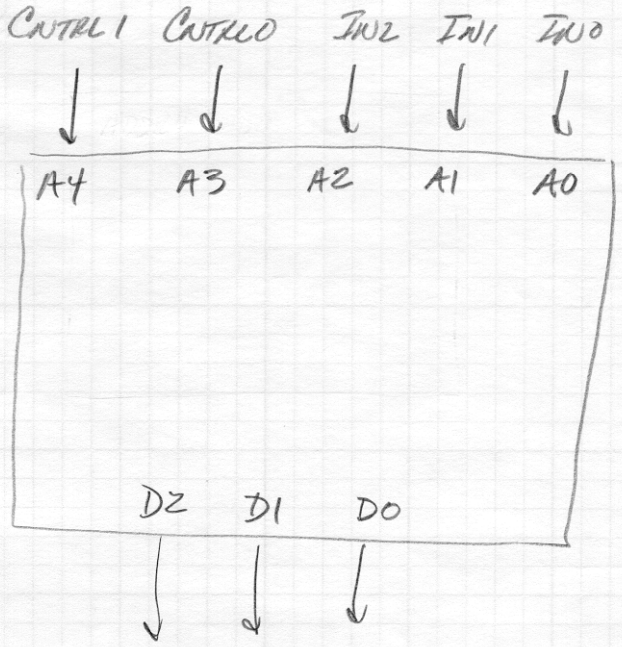
In this problem you are asked to design a circuit that takes as its input, a three bit number (In2, In1, In0) and produces its complement (Out2, Out1, Out0). The input number can be in unsigned, sign magnitude, 1's complement or 2's complement representation. A 2-bit control input (Cntrl1, Cntrl0) indicates the representation of the input number as follows:

Cntrl1, Cntrl0 = 00 = unsigned
01 = sign magnitude
10 = 1's complement
11 = 2's complement

If the number is unsigned, the output of the circuit is the number itself (it has no complement). In all other cases, the output should be the complement of the input in the appropriate representation.

1. Implement the design using a ROM. Define the contents of each ROM location and clearly indicate how the ROM address is constructed.

- 5 INPUT BITS CNTRL 1, CNTRL 0, IN2, IN1, IN0
- USE 32 x 3 ROM
- MOST SIGNIFICANT 2 BITS ARE CNTRL 1, CNTRL 0
- LEAST SIGNIFICANT 3 BITS ARE IN2, IN1, IN0



CNTRL1, CNTRL0 = 00 ⇒ UNSIGNED
A4, A3 = 00 (ADDRESSES 0 -7)

A2	A1	A0	D2	D1	D0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

CNTRL1, CNTRL0 = 01 ⇒ SIGN MAGNITUDE
A4, A3 = 01 (ADDRESSES 8 -15)

A2	A1	A0	D2	D1	D0
0	0	0	1	0	0
0	0	1	1	0	1
0	1	0	1	1	0
0	1	1	1	1	1
1	0	0	0	0	0
1	0	1	0	0	1
1	1	0	0	1	0
1	1	1	0	1	1

CNTRL1, CNTRL0 = 10 ⇒ 1's COMPLEMENT

A4, A3 = 10

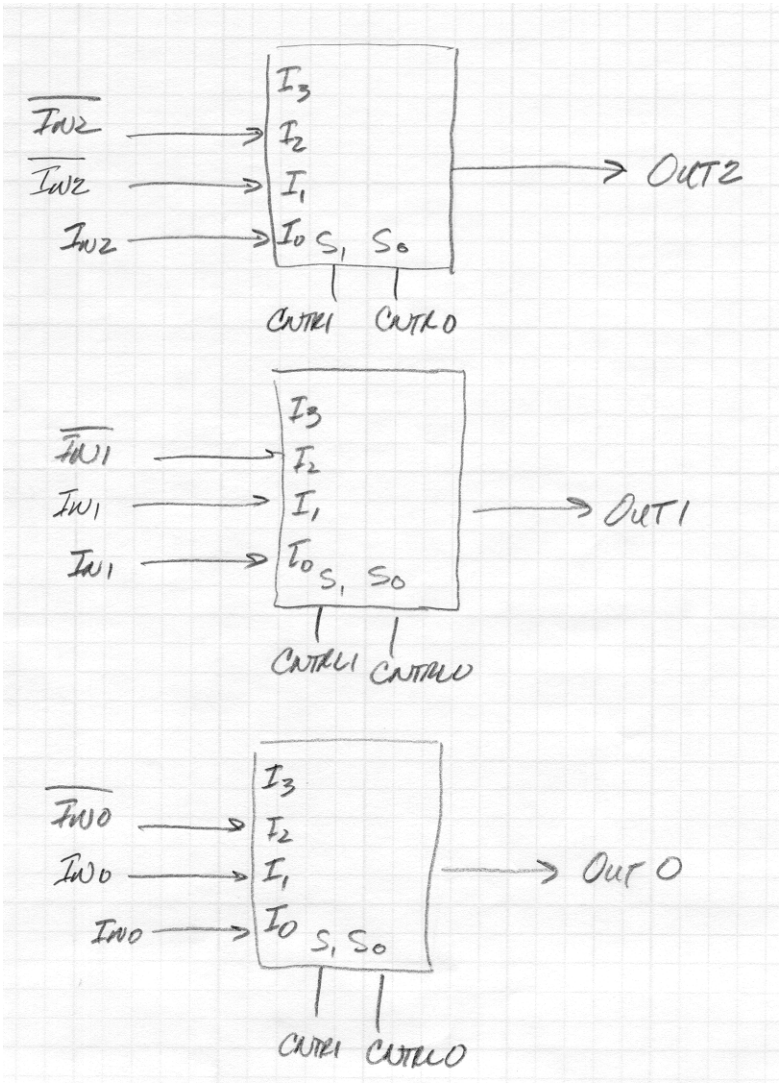
A2	A1	A0	D2	D1	D0
0	0	0	1	1	1
0	0	1	1	1	0
0	1	0	1	0	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	0	1	0
1	1	0	0	0	1
1	1	1	0	0	0

CNTRL1, CNTRL0 = 11 ⇒ 2's COMPLEMENT

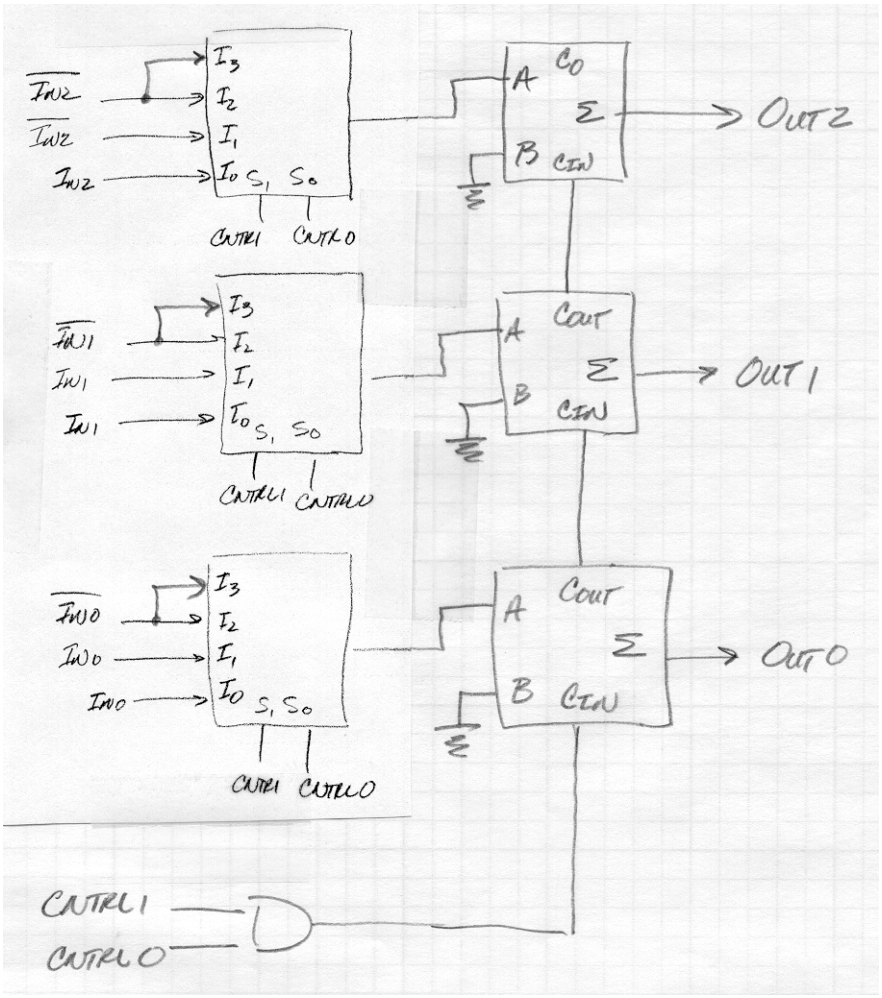
A4, A3 = 11

A2	A1	A0	D2	D1	D0
0	0	0	0	0	0
0	0	1	1	1	1
0	1	0	1	1	0
0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	0	1	1
1	1	0	0	1	0
1	1	1	0	0	1

2. Ignoring (for the moment) the 2's complement portion of the design (Cntrl1, Cntrl0 = 11), redesign the circuit using 3, 4-to-1 multiplexers (i.e., generate the unsigned, sign magnitude and 1's complement numbers). You can assume that both the true and complemented versions of In2, In1 and In0 are available (no inverters are necessary)



3. Adding three full adders and a single AND gate to the design in part 2, complete the design to generate the 2's complement of the number (Cntrl1, Cntrl0 = 11).



Problem #4.

In this problem you are to design a two-bit, combinational comparator. The circuit has two, two-bit inputs A (A1, A0) and B (B1, B0) and three outputs A<B, A=B and A>B. Assume both A and B are unsigned integers and can take on the values 0 through 3. A1 and B1 are the more significant bits.

1. Design the circuit using an appropriately sized ROM. Show the contents of each memory location in the ROM.

ROM IS 16 x 3

A1	A0	B1	B0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

2. Design the circuit using a decoder with high true outputs (again, of the appropriate size) and OR gates. Use sum of minterm notation in constructing your solution.